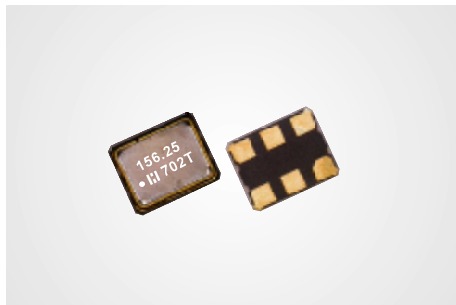


D3ST Series

3225 LVDS OSC



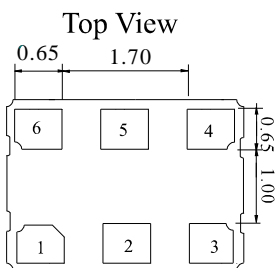
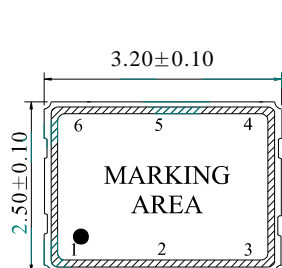
FEATURES

- 3.2*2.5*1.2mm package
- Tri-State function available
- Low Jitter and Noise
- LVDS output
- Ideal for Fiber-optic communication applications, FTTH and SONET/SDH applications, Sever, FCHBA, Fibre Channel, Gigabit Ethernet, and Serial ATA

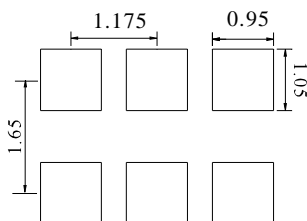
Electrical Specifications

Parameter	Condition	D3ST	
Frequency Range	F ₀	25~212.5MHz	
Output Specification		LVDS	
Frequency Stability*	All Condition	± 25ppm, ± 50ppm, ± 100ppm	
Operating Temperature Range	T _{OPR}	-20°C~+70°C (-40°C~+85°C option)	
Storage Temperature Range	T _{STG}	-55°C~+125°C	
Power supply Voltage	V _{DD}	3.3V+/-5%	2.5V+/-5%
Supply Current	I _{DD}	80mA Max	
Output Symmetry	Sym	At ½V _{pp} 40/60%(45/55% Option)	
Rise time	T _r	20%V _{pp} ~80%V _{pp}	1nS Max
Fall Time	T _f	80%V _{pp} ~20%V _{pp}	1nS Max
Output Voltage	V _{OH} V _{OL}		1.4V Typ. 1.1V Typ.
Differential output voltage	V _{OD}		350mV Typ.
Differential output error	ΔV _{OD}		40mV Typ.
Offset voltage	V _{OS}		1.25V Typ.
Offset error	ΔV _{OS}		50mV Typ.
Output Load		100 Ω Ouput - comp. output	
Integrated phase jitter (RMS)	Integrated 12KHz to 20MHz	1pS Max	
Start Time	T _s	10mS Max	
Aging(First Year)	25°C ± 3°C	± 2ppm Max	
Pin 1, tri-state function		Pin 1=H or open....Output active at pin 4,5 Pin 1=L.....high impedance at pin 4,5	
Packing Unit		3000pcs/reel	

Mechanical Dimensions(mm)

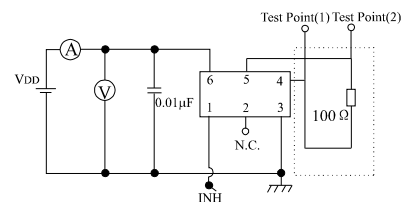


Recommended Solder Pattern

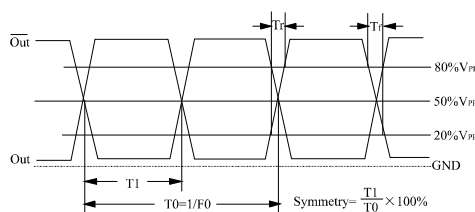


Pin	Connection
#1	Tri-State
#2	N.C.
#3	GND
#4	Comp. Output
#5	Out
#6	V _{DD}

Test Circuit



Output Waveform



**Note: 0.01uF bypass capacitor should be placed between V_{DD}(Pin6) and GND(Pin3) to Minimize power supply line noise