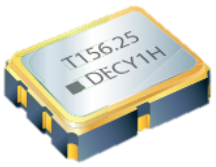
Product Features

1. 6 pads seam sealed ceramic package
2. Supply Voltage ： 1.8 , 2.5 , 3.3V (Typ.)
3. Output Type ： LVPECL / LVDS / HCSL
4. Excellent low phase noise and jitter
5. High Power Supply Noise Rejection Performance
6. Tri-State function available
7. RoHS and REACH Compliant , Pb-free , Halogen-free
8. AEC-Q200/AEC-Q100 Compliant.
9. Industry Standard Package ：
   3.2 x 2.5 x 0.95 mm

Application ：

- Automotive Infotainment
- Automotive Communication
- Automotive Safety
- Automotive Security
- Automotive ADAS



Test condition
Ambient temperature：25 ± 5℃
Relative humidity： 40% ~ 70%

- **Table 1 . Electrical Specifications**

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions & Notes
LVPECL / LVDS / HCSL Common Electrical Characteristics						
Nominal Frequency	F		25 ~ 320		MHz	3rd Overtone
Frequency Stability	ST		± 25		ppm	@ -40~85℃ , Note 1
			± 35			@ -40~105℃ , Note 1
			± 75			@ -40~125℃ , Note 1
Operating Temperature	Topr	-40	-	85	℃	
		-40	-	105		
Supply Voltage	Vdd		1.8 , 2.5 , 3.3 (± 10%)		V	
Symmetry	TH/T	45	50	55	%	
Start-up Time	Tosc	-	-	10	ms	To 90% of Final Amplitude
LVPECL Electrical Characteristics						
Current Consumption	Icc	-	-	40	mA	RL=50Ω to VDD-2V
Standby Current	Icc(ST)	-	-	20	uA	OE = Low
Output Voltage High	VoH	VDD-1.025	-	VDD-0.74	V	
Output Voltage Low	VoL	VDD-1.81	-	VDD-1.405	V	
Output Voltage Range	Vdiff	600	1400	2000	mV	Differential Peak-to-Peak
Rise / Fall Time	Tr / Tf	-	-	0.5	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7VDD	-	-	V	Note 2 , (Logic 1)
Enable Voltage Low	-	-	-	0.3VDD	V	Note 2 , (Logic 0)
Output Enable Delay Time	-	-	-	2	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	-	0.1	ps	Integrated from 12KHz ~ 20MHz @156.25MHz , 3.3V , Note3

Test condition
Ambient temperature：25 ± 5℃
Relative humidity： 40% ~ 70%

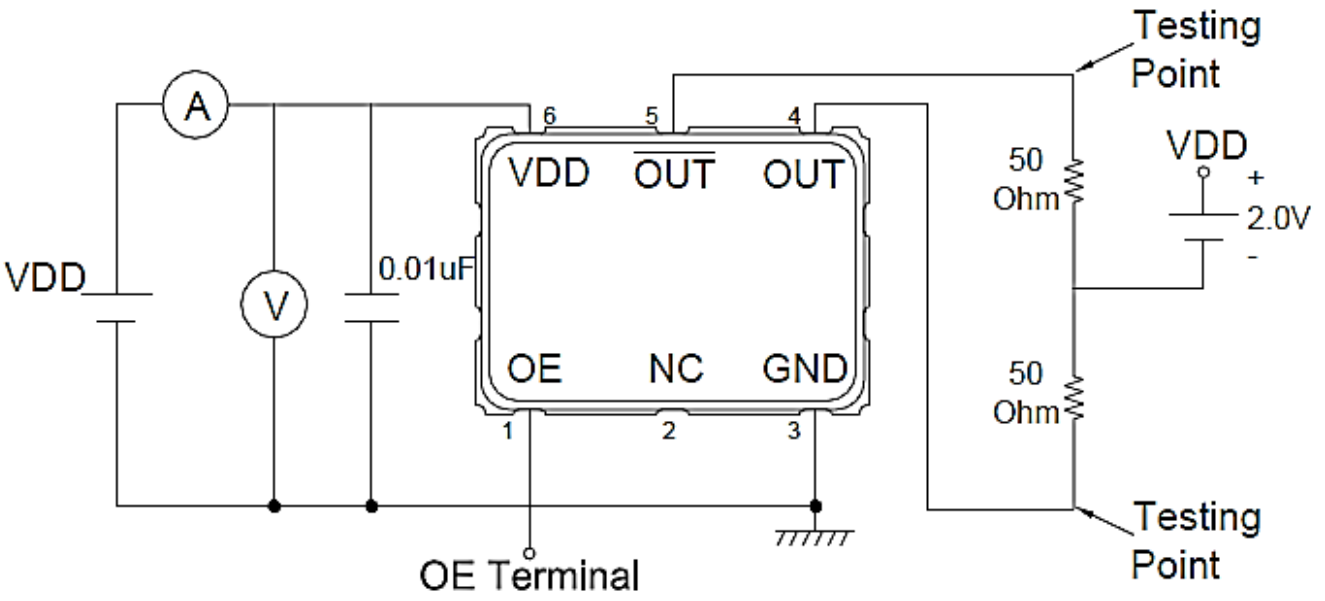
- **Table 1 . Electrical Specifications (continued)**

Parameters	Symbol	Min.	Typ.	Max.	Units	Notes
LVDS Electrical Characteristics						
Current Consumption	Icc	-	-	40	mA	RL=100Ω
Standby Current	Icc(ST)	-	-	15	uA	OE = Low
Output Voltage High	VoH	-	1.43	1.6	V	
Output Voltage Low	VoL	0.9	1.1	-	V	
Offset Voltage	-	1.125	1.250	1.375	V	
Output Swing (Single)	-	247	330	454	mV	Single Peak-to-Peak
Output Swing (Differential)	Vdiff	494	660	908	mV	Differential Peak-to-Peak
Rise / Fall Time	Tr / Tf	-	-	0.35	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7VDD	-	-	V	Note 2
Enable Voltage Low	-	-	-	0.3VDD	V	Note 2
Output Enable Delay Time	-	-	-	2	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	-	0.2	ps	Integrated from 12KHz ~ 20MHz @156.25MHz , 3.3V , Note3
HCSL Electrical Characteristics						
Current Consumption	Icc	-	-	30	mA	RL=50Ω
Standby Current	Icc(ST)	-	-	10	uA	OE = Low
Output Voltage High	VoH	660	740	850	mV	
Output Voltage Low	VoL	-150	0	150	mV	
Rise / Fall Time	Tr / Tf	-	-	0.5	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7VDD	-	-	V	Note 2
Enable Voltage Low	-	-	-	0.3VDD	V	Note 2
Output Enable Delay Time	-	-	-	2	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	-	0.2	ps	Integrated from 12KHz ~ 20MHz @100MHz , 3.3V , Note3

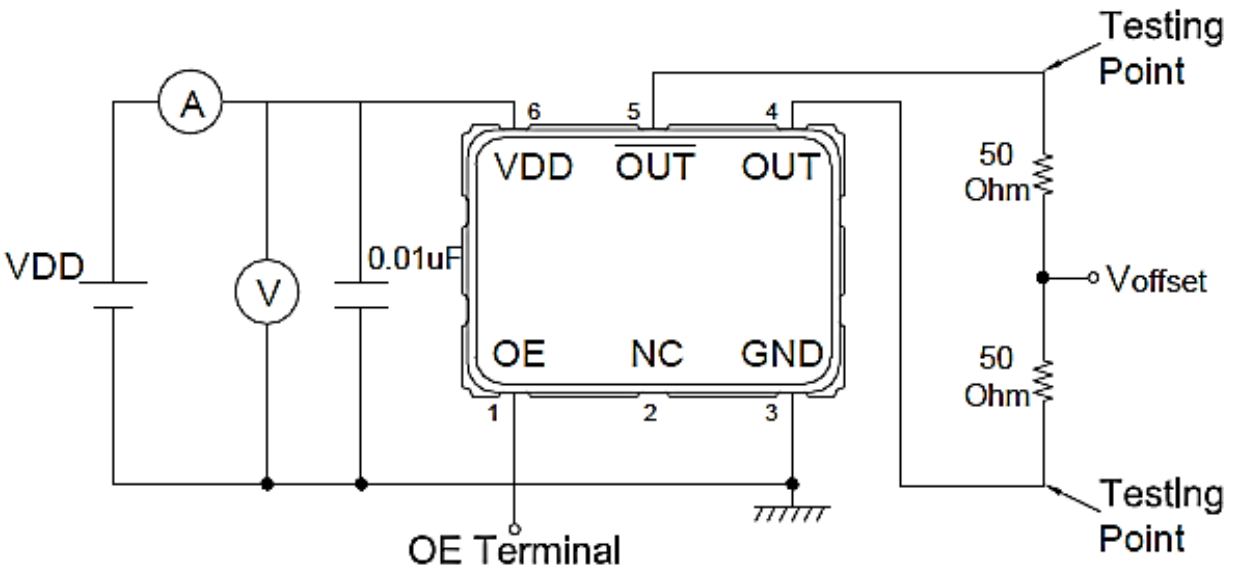
Note 1 : Inclusive of frequency tolerance at 25℃ , variation over temperature , supply voltage variation , 10 years aging and vibration.
Note 2 : Output will be enable if OE is Logic 1 or open ; Output will be disable if OE is Logic 0.
Note 3 : Phase Jitter will be slightly different according to output frequency and supply voltage.

- **Test Diagram**

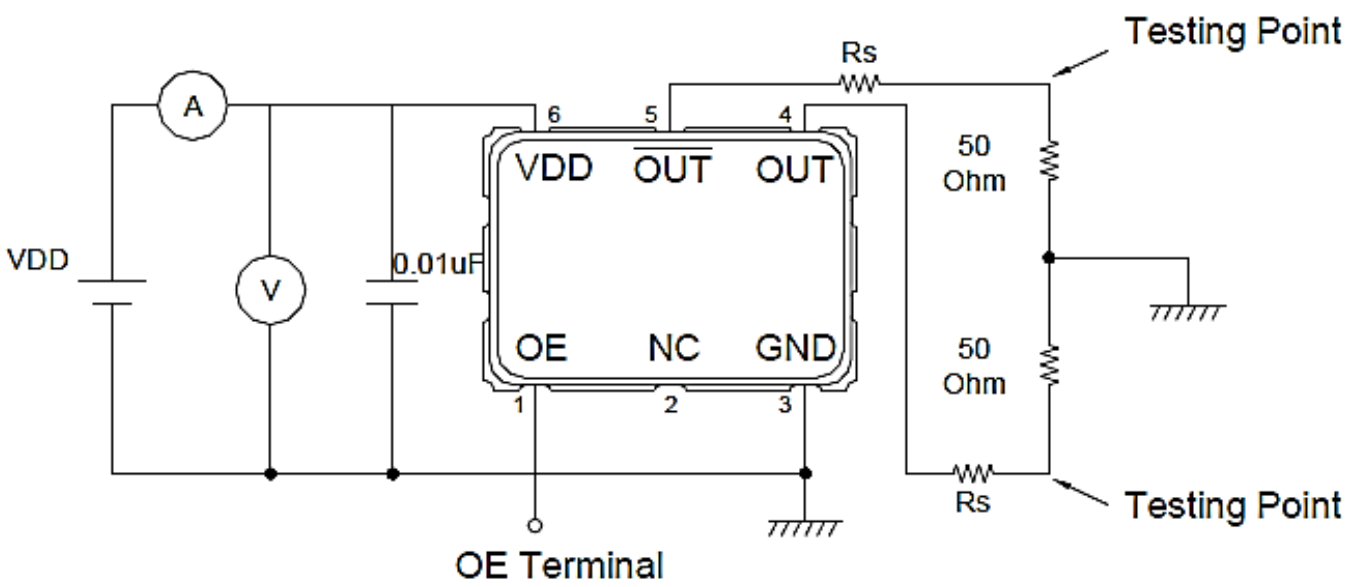
■ LVPECL



■ LVDS



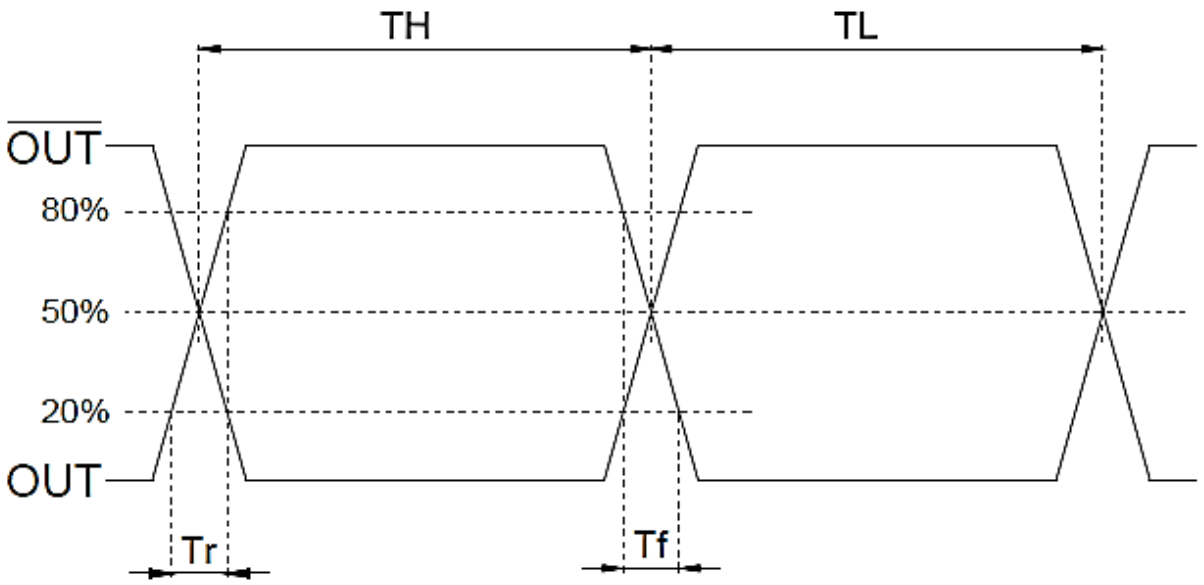
■ HCSL



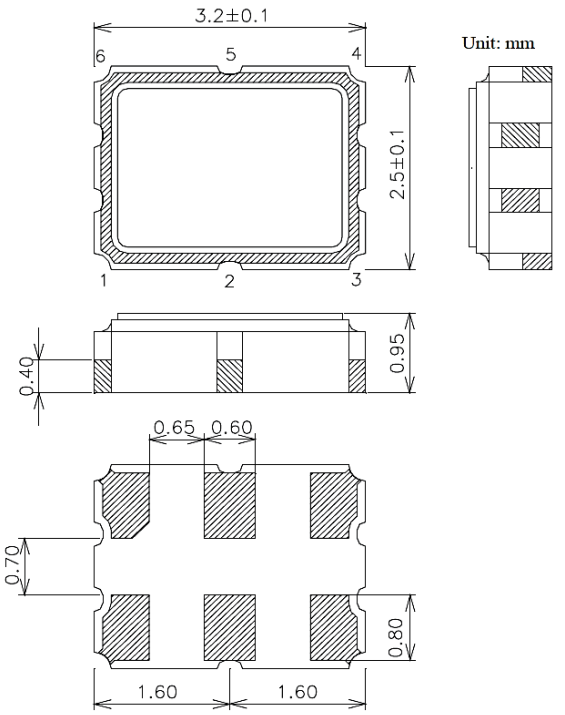
Testing Circuit Note:

1. Above testing circuits cover all the specifications except temperature test & Jitter measurement.
2. All the testing equipment are 50 Ohm terminal.
3. OE terminal is open connection except OE function test.
4. RS= 0 Ohm for test. 0 Ohm to 33 Ohm to minimize overshoot and ring back effect in application.

- Waveform **Conditions**



- **Dimensions & Footprint (Recommended)**

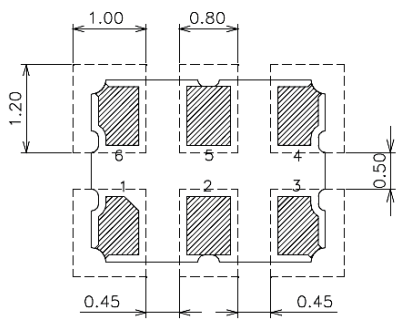


※ Pad dimension tolerance ±0.2 mm

Pin Function:

1. OE
2. NC
3. GND
4. OUT
5. $\overline{OUT}$
6. VDD

Land Pattern:



※ Power Supply Decoupling Capacitor is Required.